CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of fabricating an electronic chip on a wafer, comprising:

developing on a surface of said wafer a first mask at a predetermined lower resolution; and

etching said first mask under a first set of conditions for a predetermined period to achieve a higher resolution mask.

2. The method of claim 1, wherein said first mask comprises of organic photo-sensitive resist material.

3. The method of claim 1, wherein said first set of conditions comprises an oxygen and nitrogen plasma etch, wherein

a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;

a setting of an RF power is in the range of 50 to 200 watts; and

a setting of a presssure is between 10 and 45 mTorr.

4. The method of claim 1, further comprising:

etching, under a second set of conditions for a second predetermined period, at least one layer of said wafer or at least one layer of material deposited on said wafer, to remove at least a portion of said at least one layer to produce features at said higher resolution.

5. The method of claim 4, wherein said second set of conditions comprises a CF_4/ CHF_3/ Argon based hard-mask process for etching a gate oxide layer.

6. The method of claim 5, wherein said second set of conditions further comprises a range of 20-80 sccm (standard Cubic Centimeters/Minute) for CF_4, 5-15 sccm for CHF_3, and 40-200 sccm for argon.

7. A method of fabricating at least one electronic device or circuit on a wafer, comprising:

developing a first mask on an outer surface of said wafer or of a layer of material deposited on said surface to define a pattern for at least part of a structure or circuit component for said electronic device or circuit, said first mask comprising an organic photo-sensitive resist material;

performing a trimming process on said first mask to adjust dimensions of

said pattern; and

using said trimmed first mask as a hard mask for an etching process to remove material from at least one layer below said hard mask.

8. The method of claim 7, wherein said trimming process of said first mask comprises an oxygen and nitrogen plasma etch, wherein

a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;

a setting of an RF power is in the range of 50 to 200 watts; and

a setting of a presssure is between 10 and 45 mTorr.

9. The method of claim 7, wherein said etching process to remove material from said at least one layer below said hard mask comprises a CF_4/ CHF_3/ Argon based hard-mask process for etching a gate oxide layer.

10. The method of claim 9, wherein conditions of said etching to remove material off at least one layer below said hard mask comprises a range of 20-80 sccm (standard Cubic Centimeters/Minute) for CF_4, 5-15 sccm for CHF_3, and 40-200 sccm for argon.

11. A method of controlling line width variation tolerances during fabrication of electronic devices or circuits on a wafer, comprising:

developing a first mask on an outer surface of said wafer or of a layer of material deposited on said surface to define a pattern for at least part of a structure or circuit component for said electronic device or circuit, said first mask comprising an organic photo-sensitive resist material;

performing a trimming process on said first mask to adjust dimensions of features of said first mask; and

using said trimmed first mask as a hard mask for an etching process to remove material from at least one layer below said hard mask.

12. A method, during fabrication of electronic devices or circuits on a wafer, said devices or circuits having both isolated features and nested features, of controlling line width variation tolerances of said isolated features relative to said nested features while independently achieving a target critical dimension, comprising:

establishing a first set of conditions for an RF etch process that achieves said target critical dimension; and

controlling a level of said RF power as a parameter to independently control said line width variation tolerance of said isolated features relative to said

nested features.

13. An electronic device or circuit fabricated at least in part by the method defined in claim 1.

14. An electronic device or circuit fabricated at least in part by the method defined in claim 7.

15. An electronic device or circuit fabricated at least in part by the method defined in claim 11.

16. An electronic device or circuit fabricated at least in part by the method defined in claim 12.